

FIG. 1

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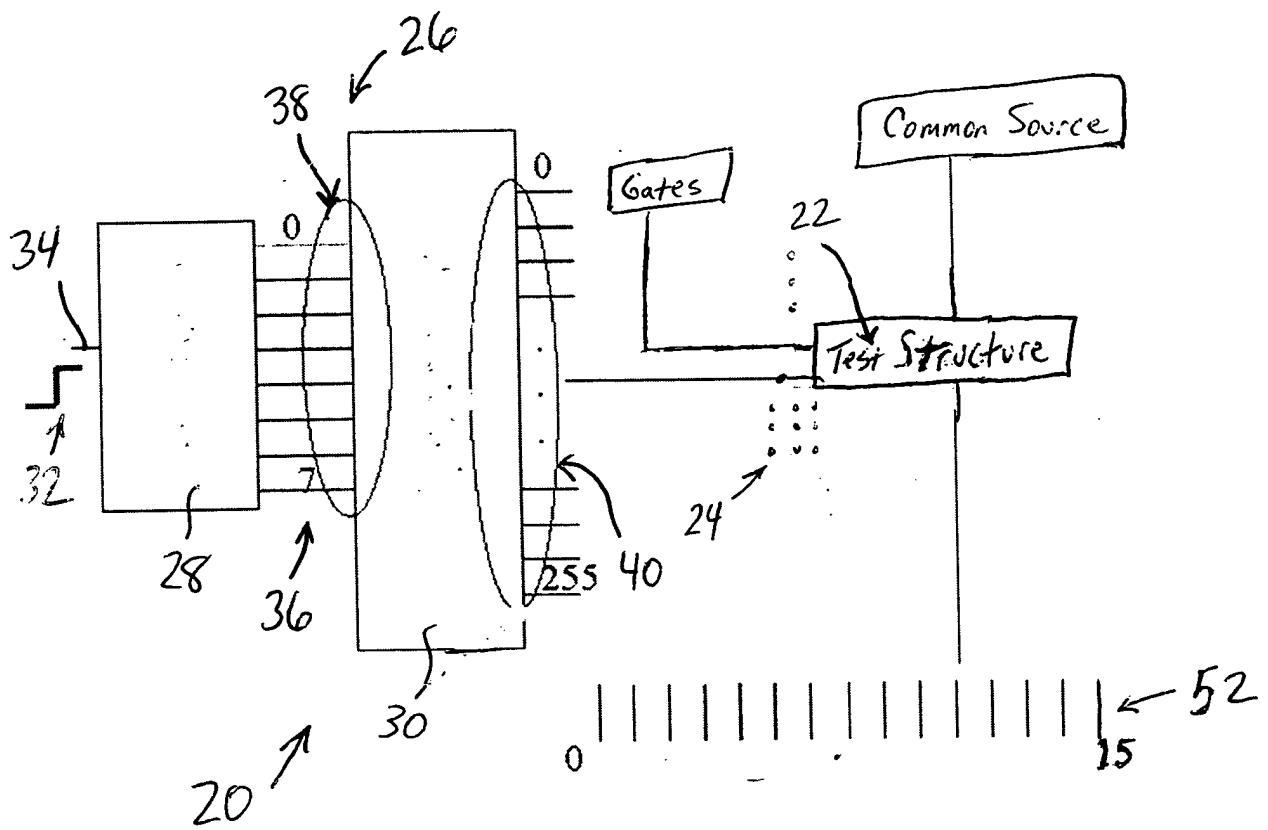


FIG. 2

Outputs Trigger	7	6	5	4	3	2	1	0
1 st	0	0	0	0	0	0	0	1
2 nd	0	0	0	0	0	0	1	0
3 rd	0	0	0	0	0	0	1	1
			
256 th	1	1	1	1	1	1	1	1

FIG. 3

44 46
42
48

Input Seq. →	1 st	2 nd	3 rd		256 th
0	0	1	0		1
1	0	0	1		1
2	0	0	0		1
3	0	0	0	• • •	1
4	0	0	0		1
5	0	0	0		1
6	0	0	0		1
7	0	0	0		1

inputs:
address
lines

FIG. 4

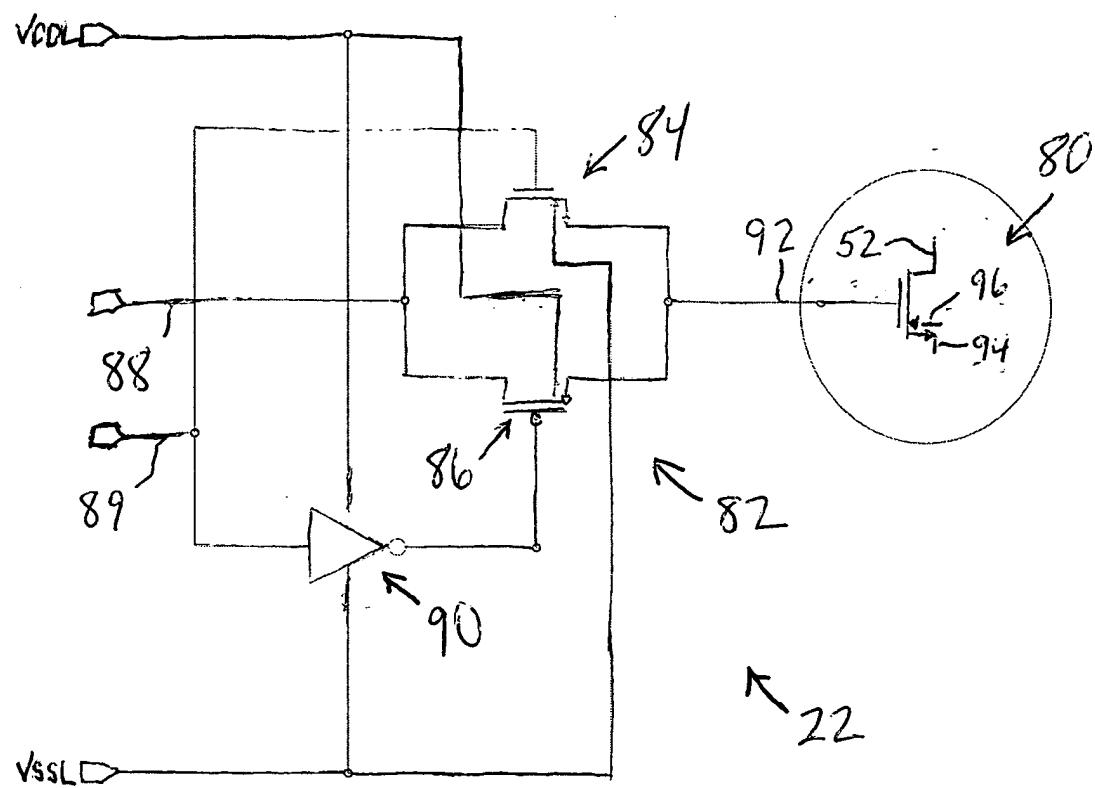


FIG. 5